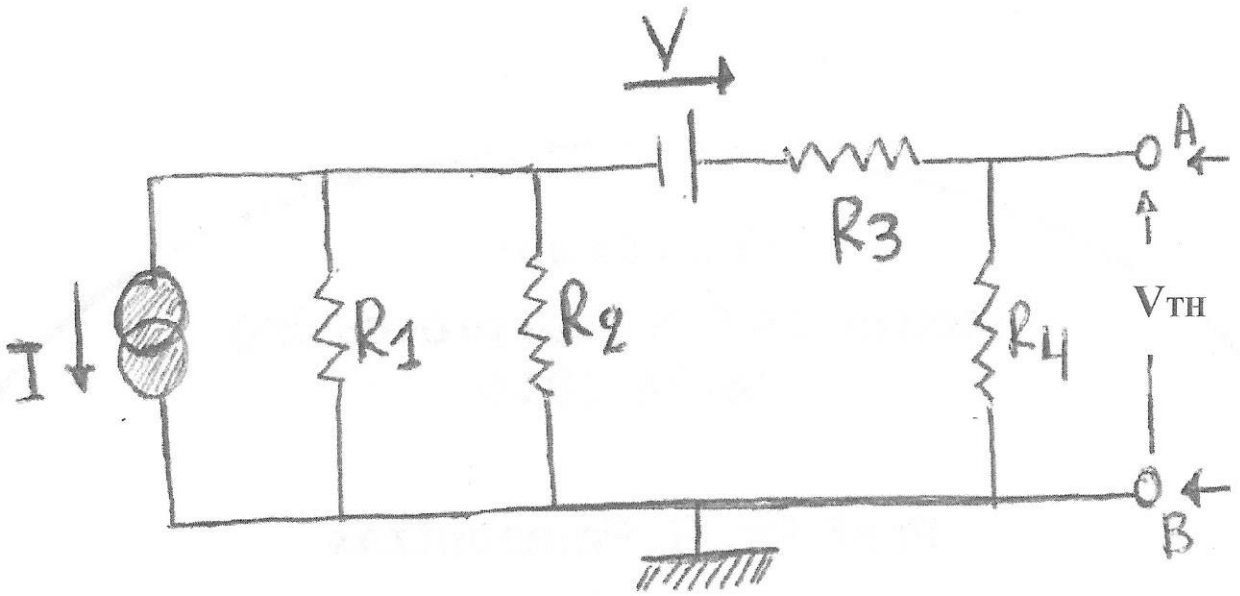
Final exam
Electronics & Signal processing
06-04-2016

Prof. Dr. G. Palasantzas

Grade of written exam:
Mark is cummulative points scored for all problems
Total maximum score : 10

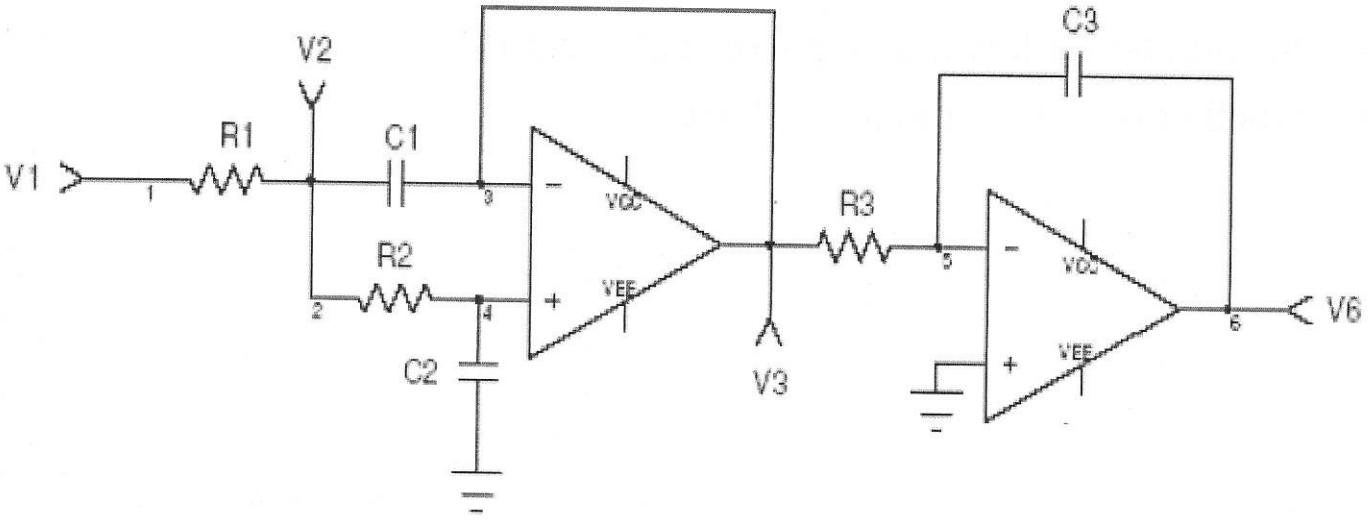
Problem 1 (1.5 points)



Derive the Thévenin equivalent between points A and B by calculating the Thévenin potential **VTH** (1 point) and the Thévenin resistance **RTH** (0.5 points) using only the Thevenin-Norton concepts to analyze the circuit.

Problem 2 (2.5 points)

Consider the circuit below with two ideal opamps (**V+=V-**)



(a: 0.5 points) Show that : $\frac{V(6)}{V(3)} = -\frac{1}{j\omega\tau_3}$

where $\tau_3 = R_3C_3$.

(b: 1.5 points) Show that

$$V(2) = \frac{(\frac{R_1}{R_2} + j\omega\tau_1)\, V(3) + V(1)}{1 + \frac{R_1}{R_2} + j\omega\tau_1}$$

where $\tau_1 = R_1C_1$.

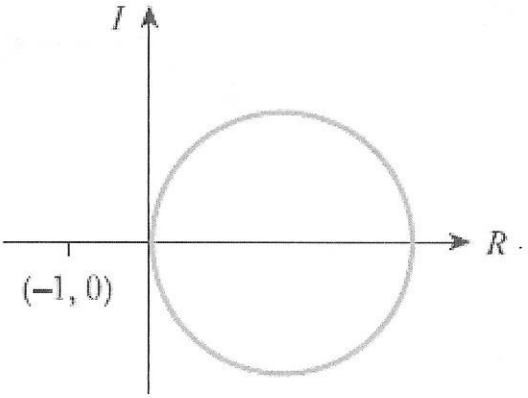
(c: 0.5 points) Show that $V(3) = V(4) = \frac{V(2)}{1 + j\omega\tau_2}$

where $\tau_2 = R_2C_2$.

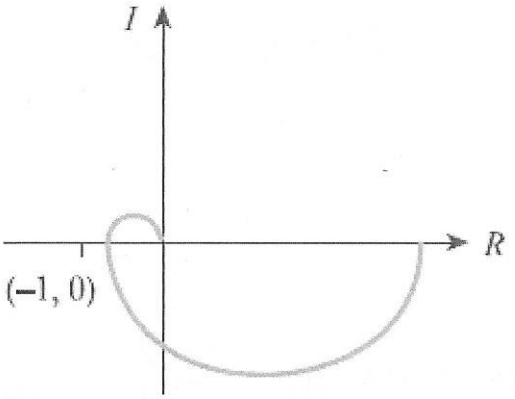
Problem 3 (1 point)

The Nyquist diagrams below represent four circuits (0.25 points per circuit). In each case determine:

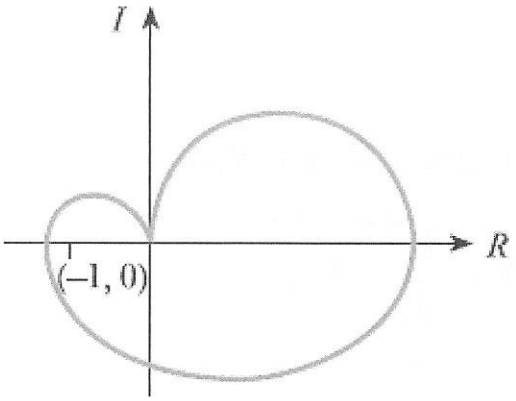
- the number of low and high-frequency cut-offs
- whether or not the circuit is stable.



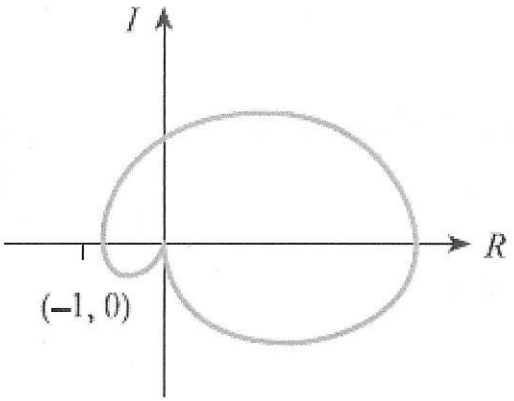
(a)



(b)



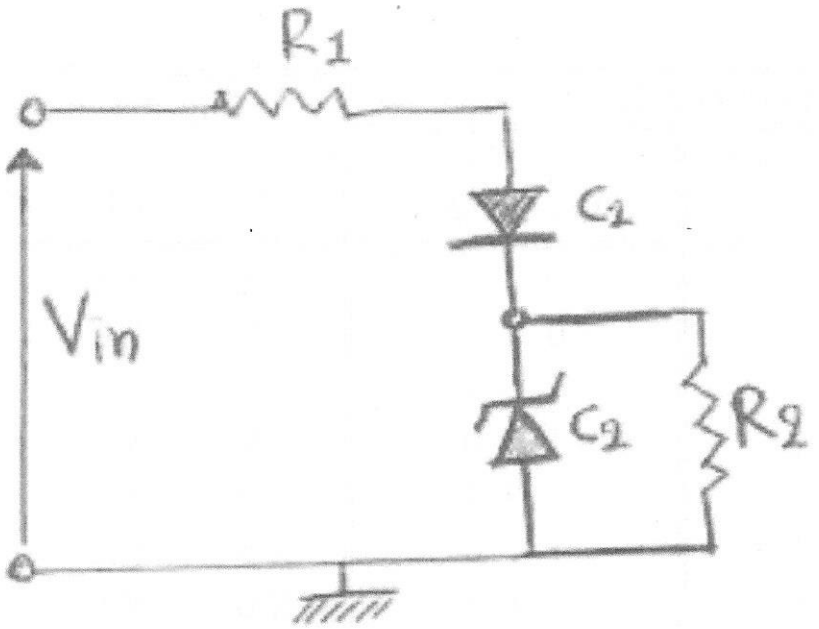
(c)



(d)

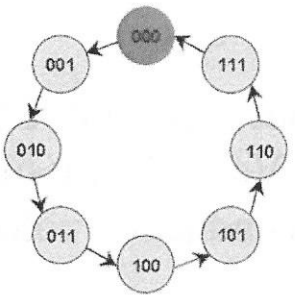
Problem 4 (1.5 points)

The diodes C1 and C2 are assumed ideal with forward conduction voltage Vc <<Vin (>0). The Diode C2 is also a Zener diode with reverse conduction voltage Vz (<<Vin).



Calculate the current through the resistor R2 and discuss possible restrictions for the resistor ratio R1/R2 depending on the operation of C1 and C2.

Problem 5 (2 points)



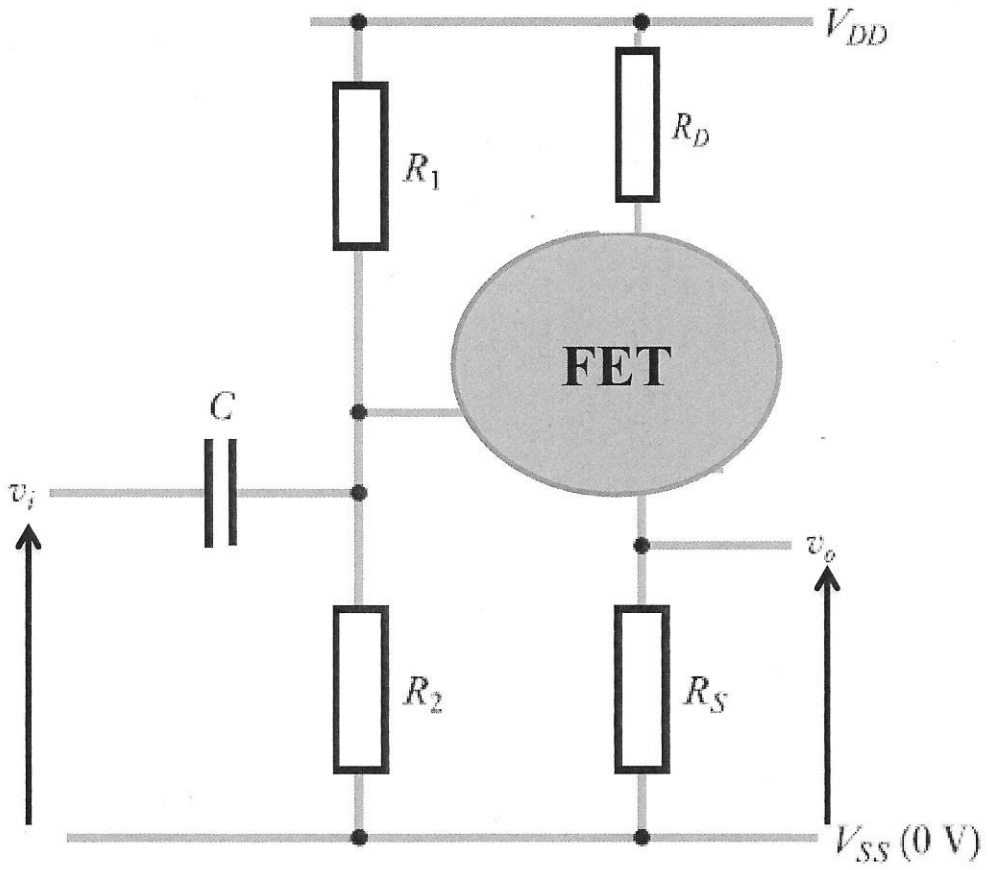
(a: 1 point) Using the output table given below, design the synchronous 8-counter 0→7 (X: do not care) using 3 J-K flip-flops:

Output State Transitions		Flip-flop inputs		
Present State Q2 Q1 Q0	Next State Q2 Q1 Q0	J2 K2	J1 K1	J0 K0
0 0 0	0 0 1	0 X	0 X	1 X
0 0 1	0 1 0	0 X	1 X	X 1
0 1 0	0 1 1	0 X	X 0	1 X
0 1 1	1 0 0	1 X	X 1	X 1
1 0 0	1 0 1	X 0	0 X	1 X
1 0 1	1 1 0	X 0	1 X	X 1
1 1 0	1 1 1	X 0	X 0	1 X
1 1 1	0 0 0	X 1	X 1	X 1

(b: 1 point) Using the result from (a) identify J-K flip-flops acting as internal clocks in order to design a simpler version of the synchronous 8-counter (asynchronous).

Problem 6 (1.5 points)

Consider a FET as shown bellow:



Show that the amplification ratio of the input/output potential variations υo/υi is given by:

$$\frac{\upsilon_o}{\upsilon_i} = \frac{g_m R_s}{1 + g_m R_S + [(R_D + R_S)/r_d]}$$

with g_m the transconductance and r_d the differential resistance of the FET operating at saturation.